AMENDMENTS TO THE SPECIFICATION

On page 4, please amend Paragraph **[0015]** as shown below:

[0015] ~~Fig. 7 illustrates~~ Figs. 7A-7E are cross-sectional views of structures to illustrate a nano-imprint process used to create a photonic crystal pattern on a wafer, starting with the structure in Fig. 1.

On page 6, please amend Paragraph **[0018]** as shown below:

[0018] ~~Layer 124~~ Layer 124' in Fig 1 is a contact layer to provide a transition to an ultra thin metal layer 125, which is followed by an Indium Tin Oxide (ITO) layer 126. ITO layer 126 and Ultra thin metal layer 125 are used to increase current spreading over the wafer surface. Current spreading layers for LEDs are described in U.S. ~~patent application, Ser. No. 10/641,641, filed Aug. 14, 2003, which application~~ Patent No. 6,958,494, which patent is incorporated by reference herein in its entirety. The ITO is transparent and conductive and its index of refraction is about 1.8. It also acts as an antireflection coating to reduce the Fresnel reflection at the air interface or the interface to external media such as encapsulating epoxy. Generally the Fresnel reflection at semiconductor epitaxial-air interface is high due to high index of semiconductor materials, which results in about 17 % reflection at GaN-based material-air interface and 30 % reflection at GaAs-based material-air interface. Therefore the ITO layer 126 plays a significant role on enhancing the optical output. Other conductive and transparent material, which has index of refraction lower than those of semiconductor layers, can be used to replace ITO as the material used for the current spreading layer which also reduces Fresnel reflection.

On page 8, please amend Paragraph **[0021]** as shown below:

[0021] Fig. 2 shows that the holes 201 are drilled from the top of the wafer. But when the wafer bonding technique is used, the holes can be imbedded from layers 131 or 123 or even through the active layer 121 into waveguide layer 122 and cladding layer 124. Wafer bonding technique is to flip over the epitaxial structure by taking out the original substrate such as 110 and then bond a new substrate on the original top layer such as the ~~layer 124~~ layer 124' if the

ITO layer 126 in Fig. 2 is omitted. If the new substrate has a band gap that is wider than that of the active layer, the photons emitted by the active layer will not be significantly absorbed by the new substrate, so that light can be emitted from both sides of the solid state light emitting system. This may be advantageous for some applications. For example, where GaAs is the material in the original substrate for the solid state light emitting system, a material with a band gap that is wider than that of GaAs may be used, such as GaP.

On page 10, please amend Paragraph **[0025]** as shown below:

[0025] Inside the chip, the geometrical shapes of photonic crystal cells and electrodes can be arranged in many ways for the sake of optimizing optical and electrical performance of the solid state light emitting chip. Fig. 5 shows an example of hexagonal PC cells arranged in a chip. The hexagonal shape allows the photonic crystal to interact photons from all directions more effectively. Hexagonal cells are surrounded by electrode network 520 (white area in Fig. 5). As in the case of Figs. 3A-3D, since the hexagonal-shaped openings in the electrode (each opening in the electrode exposing a corresponding hexagonal PC cell) are arranged in a periodic array, arrays of network cells 316' of the electrode that are substantially similar to one another can be defined for the electrode in Fig. 5 as well. The term "network cell" therefore can be defined to encompass both the grid cells 316 of Figs. 3A-3D and those (316') of Fig. 5. The wire connected to the electrical power source can be bonded at 510 or at the edge 511. According to the theoretical calculation for the optimal performance for the case of no holes beneath the electrode 520, the electrode width W between two adjacent hexagonal cells is preferably approximately equal to ~~$\sqrt{3}$ a, where a~~ $\sqrt{3}$ b, where b is the length of a side of the hexagon. Fig. 6 shows the triangular array of holes fitting into a hexagonal PC cell. Other shape arrangements are feasible and within the scope of the present invention.

On page 11, please amend Paragraph **[0027]** as shown below:

[0027] ~~Fig. 7 illustrates~~ Figs. 7A-7E illustrate the nano-imprint process and its associated etching. As indicated above, the PC cells comprise holes of very small dimensions, which holes can be formed using the nano-imprint process of ~~Fig. 7.~~ Figs. 7A-7E. The mold for making the nano-imprint in the Step 1 can be made by either electron beam lithography or Optical

lithography. In the present invention, electron beam lithography is preferably used to make a mold with protruded nano-scale cylindrical pillars (positive mold) or nano-scale recessive holes (negative mold). Negative mold is used to replicate positive daughter molds for printing. For example, electron beam lithography or Optical lithography may be used to first make a negative mold, which is used in turn to replicate positive daughter molds that are actually used for the printing process.